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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/087,826	03/05/2002	Devereaux C. Chen	0023-0052	4763

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EXAMINER	
INOA, MIDYS	
ART UNIT	**PAPER NUMBER**
2188	5

DATE MAILED: 06/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/087,826	CHEN ET AL.	
	Examiner	Art Unit	
	Midys Inoa	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-6, 8-11, and 14-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Bronson et al. (6,065,088).

Regarding Claim 1, Bronson et al. teaches a queuing system divided into two areas, an interrupt routing unit ("first queuing area") and the remaining queues ("second queuing area"). In this system, the second queuing area has the ability to receive data from the first queuing area through buses 137 and 139 (see Figure 3). The queuing system also has the ability to bypass the first queuing area by sending specific commands directly to the command queue in the second queuing area through bus 141 ("bypass logic"). When bypassing the interrupt routing unit, specific commands are being sent that do not need to go through this first queuing area, and thus, the command queue in the second queuing area should be ready to accept the data that is being sent through bus 141. Additionally, **such commands can be bypassed in an instance when the first queuing area is empty or full; therefore, in an instance where the first queuing area is empty and the commands are being bypassed, the second queuing area is ready to receive the bypassed data ("bypass logic").**

Regarding Claims 8 and 20, Bronson et al. teaches a FIFO command queue 146 receiving memory mapped input/output (MMIO) commands from a system bus control logic 140. Since

this is a FIFO queues (Microsoft Computer Dictionary, Page 187), **the data items in the command queue 146 are forwarded to the normal priority queue 148 ("buffer") via bus 147 in a first in a first out fashion. Therefore, when the command queue is empty and the normal priority queue has space for the data item, a data item that comes in to the command queue 146 will go through the command queue and then to the normal priority queue (see Figure 3).** Additionally, when the command queue is not empty, new data items are simply added to the top of the queue as older data items are de-queued and transferred to the normal priority queue via bus 147 ("enqueuing... dequeuing..."). Once an item is sitting in the normal priority queue 148, it will eventually be outputted through the I/O Bus Control logic 152 and I/O bus 102 (see Figure 3, column 8, lines 33-41).

Regarding Claim 14, Bronson et al. discloses a system (Figure 3), which **could be coupled to multiple processors via the system bus 100**. Additionally, Bronson discloses a system bus control logic 140 ("request manager") receiving memory requests through system bus 100 which are meant to be processed by processors which will receive the commands via I/O bus 102 once the commands have gone through the entire queuing system. Bronson also discloses a multiplexor 144 ("arbiter") receiving memory commands through bus 141 ("input port"), where the memory commands originate from processors in a system beyond system bus 100; the multiplexor coupled to a command queue ("a queue corresponding...") implemented as a FIFO queue. The command queue is part of a queuing area comprising normal and high priority queues, which act as buffers. When the receiving command queue is empty, the normal priority queue receives the access commands that have been forwarded from the empty queue, and when the command queue contains data items, the older data items in the command queue are de-

queued and forwarded to the normal priority queue once space is allocated. The operation of the queues is understood clearly since these queues operate as FIFO queues (Microsoft Computer Dictionary, Page 187, Figure 3, and Column 8, lines 33-41).

Regarding Claims 2, 9-10, and 21, Bronson et al. teaches the queuing to memory mapped input/output (MMIO) commands as well as memory interrupt commands. These commands affect the access of a memory, therefore, they can be considered to be a type of memory access command (Abstract and Figure 3).

Regarding Claim 3, Bronson et al. teaches an interrupt routing unit 142 ("first queuing area") divided into two parallel queues, the EOI queue 136 and the INR, IRR queue 134 ("plurality of parallel sub-queues", Figure 3).

Regarding Claims 4-5, 11, 15, and 17 Bronson et al. teaches a second queuing area which includes a normal priority queue 148 and a high priority queue 150 which act as independent buffers ("first buffer... second buffer"). In addition, Bronson et al. discloses an I/O bus control logic 152 ("encoding component"), which reads data from the priority queues, giving higher priority to the high priority queue 150, and passes on the data read to the I/O Bus 102 (Figure 3, Column 8, lines 20-32).

Regarding Claim 16, Bronson et al. teaches a queuing system with the ability to bypass the first queuing area by sending specific commands directly to the command queue in the second queuing area through bus 141 ("bypass logic"). When bypassing interrupt routing unit, specific commands are being sent that do not need to go through this first queuing area, and thus, the command queue in the second queuing area should be ready to accept the data that is being sent through bus 141.

Regarding Claims 6, 13, and 18 since the I/O Bus control logic is a controller based mechanism, it is possible for it to be composed of a controller with the ability to read more than one data item per clock cycle (Figure 3 and Column 8, lines 20-32).

Regarding Claim 19, Bronson et al. teaches a queuing system for access commands that could be used to arbiter commands from a plurality of local or remote sources or connected units, even in a networking environment, and therefore, could be part of a network router (Column 3, lines 34-44).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 22-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bronson et al. (6,065,088).

Regarding Claim 22, Bronson et al. teaches the arbiter of figure 3, which arbiters access commands through the use of multiple queues. Each queue of the arbiter, specifically the command queue 146, queue items at the beginning of the queue ("first stage") and de-queue items at the end of the queue ("last stage") due to their FIFO structure. In addition, the arbiter of figure 3 includes a plurality of queuing areas, of which the second queuing area includes a normal priority queue 148 and a high priority queue 150 which act as independent buffers ("first buffer... second buffer"). Bronson et al. also discloses an I/O bus control logic 152 ("arbitration logic"), which reads data from the priority queues, giving higher priority to the high priority

queue 150, and passes on the data read to the I/O Bus 102 (Figure 3, Column 8, lines 20-32). Bronson does not teach the use of a multiplexor connected to multiple stages of a queue, outputting selected data items, and coupled to and controlled by the I/O bus control logic 152. It would have been obvious to one of ordinary skill in the art to add a multiplexor between buses 149, 151 and the I/O control logic 152 since multiplexors are shown to be used in the selection of signals (Figure 3, reference #144) and such a component would be useful in selecting signals from either bus 149 or bus 151 (Figure 3). In adding such multiplexor, it would be connected to the ends of two output queues, however, since in a queue each stage of the queue is connected to the next stage of the queue, essentially the multiplexor would be connected to all stages of the queues.

Regarding Claim 23, Bronson et al. teaches a queuing system with the ability to bypass the first queuing area by sending specific commands directly to the command queue in the second queuing area through bus 141 ("bypass logic"). It is understood that when bypassing interrupt routing unit, specific commands are being sent that do not need to go through this first queuing area, and thus, the command queue in the second queuing area should be ready to accept the data that is being sent through bus 141.

Regarding Claim 24, Bronson et al. teaches the queuing to memory mapped input/output (MMIO) commands as well as memory interrupt commands. It is understood that since these commands affect the access of a memory, they can be considered to be a type of memory access command (Abstract and Figure 3).

Regarding Claim 25, Bronson et al. discloses a queuing system in which the command queue is implemented as a FIFO queue (Column 8, lines 33-36).

Allowable Subject Matter

5. Claims 7 and 12 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding Claim 7, the Prior Art of Record does not teach masking logic coupled to output buffers and configured to restore requests that were not read from the output buffers in combination with a queue system divided in to multiple queuing areas of which the second area contains two output priority buffers.

Regarding Claim 12, the Prior Art of Record does not teach moving data from a second low priority buffer to a first high priority buffer when such high priority buffer is free to receive new items. Bronson et al. (6,065,088) teaches outputting data from the low priority output queue 148 through bus 149 only when the high priority queue 150 has been emptied through bus 151. The data in the low priority queue 148 is never moved to the high priority queue 150 (Figure 3).

Response to Arguments

6. Applicant's arguments filed on April 7th, 2004 have been fully considered but they are not persuasive.

Regarding Claim 1, applicant argues that Bronson et al. does not teach the bypass logic of the invention. Bronson discloses a system in which **commands can bypassed a first queuing area in an instance when the first queuing area is empty or full; therefore, in an instance where the first queuing area is empty and the commands are being bypassed, the second queuing area is ready to receive the bypassed data ("bypass logic").**

Regarding Claims 8 and 20, applicant argues that Bronson does not disclose forwarding of commands. In the system of Bronson et al. **the data items in the command queue 146 are forwarded to the normal priority queue 148 ("buffer") via bus 147 in a first in a first out fashion. Therefore, when the command queue is empty and the normal priority queue has space for the data item, a data item that comes in to the command queue 146 will go through the command queue and then to the normal priority queue (see Figure 3).**

Regarding Claim 14, applicant argues that Bronson does not disclose a plurality of parallel processors configured to receive the memory requests from the request manager. Bronson et al. discloses a system (Figure 3), which **could be coupled to multiple processors via the system bus 100**.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Midys Inoa whose telephone number is (703) 305-7850. The examiner can normally be reached on M-F 7:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Midys Inoa

Midys Inoa
Examiner
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MI

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